REMARKS

This paper is responsive to the Final Office Action dated May 19, 2005. All rejections and objections of the Examiner are respectfully traversed. Reconsideration and further examination are respectfully requested.

At paragraphs 2-3 of the Office Action, the Examiner has now rejected independent claims 1 and 6 for anticipation under 35 U.S.C. 102(b), citing United States patent number 6,499,099 of Cho ("Cho"). Applicants respectfully traverse this rejection.

As noted in the previous Response, Cho discloses a central processing unit having an extension instruction including a memory address, an offset and a fixed length instruction of varying immediate data. The central processing unit of Cho includes a programmer accessible special register that includes an extension data field for storing extension data, or an extension register having an extension data field as one element and an extension flag that changes its status when an instruction having extension data in the extension register is executed.

Nowhere in Cho is there disclosed or suggested any method or system for manipulating data in a processor, including:

> performing a conditional shift operation on an index register based on the condition of a carry flag, the condition of the carry flag having been set by a previous arithmetic operation;
> performing an indexed load operation using the index register;
> ***wherein the conditional shift operation and the indexed load operation are performed during execution of a load-shift carry instruction***; and
> ***implementing a binary search of keys ordered in a table by executing the load-shift carry instruction.*** (emphasis added)

as in the present independent claim 1. Analogous features are also contained in the present independent claim 6. In contrast, Cho teaches performing different shift amounts in a load/store

instruction *in response to an extension flag, where the extension flag is set responsive to the receipt of an extension instruction, controls access to an extension register, and indicates the active/inactive status of the extension register*. Cho includes no hint or suggestion of any load-shift carry instruction that performs a conditional shift operation on an index register based on the condition of a carry flag, the condition of the carry flag having been set by a previous arithmetic operation, and an indexed load operation using the index register, and ***implementing a binary search of keys ordered in a table by executing the load-shift carry instruction***, as in the present independent claims 1 and 6. Cho includes no mention of performing a binary or other type of search. In contrast, the load/store instruction of Cho responds to the extension flag to accommodate different memories ("8-bit" or "16-byte"), as explained in column 10, line 33 through column 11, column 49 of Cho. Additionally, Cho includes no hint or suggestion of using a carry flag condition resulting from a previous arithmetic operation as the basis of a conditional shift operation. As previously noted, Cho includes no reference to a carry flag of any kind.

For the above reasons, Applicants respectfully urge that Cho does not disclose or suggest all the features of the present independent claims 1 and 6. Accordingly, Applicants submit that Cho does not anticipate claims 1 and 6 under 35 U.S.C. 102.

In paragraphs 4 through 19 of the Office Action, the Examiner rejected the dependent claims for obviousness under 35 U.S.C. 103, citing certain combinations of Cho with United States patents 6,157,955 of Narad et al. ("Narad et al."), 5,917,821 of Goboyan et al. ("Goboyan et al."), and United States Published Patent Applications numbers 2003/0035430 A1 of Islam et al. ("Islam et al."), and 2002/0174318 of Stuttard et al. ("Stuttard et al."). Applicants respectfully traverse this rejection.

Narad et al. disclose a packet processing system including a policy engine having a classification unit. Narad et al. teach that network packet classification, execution of actions upon those packets, management of buffer flow, encryption services, and management of Network Interface Controllers are accelerated through the use of specialized modules. Narad et al. includes a language interface for specifying both stateless and stateful classification of packets and associating actions with classification results in order to efficiently utilize these specialized modules.

Goboyan et al. disclose a look-up engine for packet-based network that parses packets in a packet-based data transmission network. A retrieving device in Goboyan et al. includes an address look-up engine having a memory storing possible values of a source field in a packet organized in a hierarchical tree structure, for performing fast look-up operations.

Islam et al. disclose a programmable network device that executes software modules resident on its hardware to support assorted applications and network management services, in which the uplink and downlink each transmit data at rates of 10 Gbps or higher. Stuttard et al. disclose a parallel data processing apparatus including a SIMD (Single Instruction Multiple Data) array of processing elements. The processing elements of Stuttard et al. are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items.

Applicants first respectfully urge that the Examiner has not established a sufficient motivation to combine the cited references. A *prima facie* case of obviousness under 35 U.S.C. 103 must include a showing of a suggestion, teaching or motivation that would have led a person of ordinary skill in the art to combine the cited references in the particular manner claimed. See In re Dembiczak, 175 F.3d 994, 998 (Fed. Cir. 1999), and In re Kotzab, 217 F.3d 1365, 1371

(Fed. Cir. 2000). In the present Office Action, the Examiner asserts that a person skilled in the art would be motivated to combine Cho with Narad et al. and Goboyan et al. "to provide a platform for accelerated network infrastructure applications by speeding up searches through lists of unknown addresses". Applicants respectfully submit that the cited references provide no hint or suggestion of any need for speeding up searches through lists of unknown address by binary searching of keys ordered in a table, such as that provided in the present independent claims 1 and 6, nor of any need for speeding up the hierarchical tree searching of addresses described in Goboyan et al.

Even if there were sufficient motivation to combine Cho with Goboyan et al. and the other references cited in paragraphs 4-19 of the Office Action, and Applicants make no admission that such motivation exists, Applicants respectfully urge that the references cited in combination with Cho in paragraphs 4 through 8 of the Office Action include no teaching or suggestion of any method or system for manipulating data in a processor, including:

> performing a conditional shift operation on an index register based on the condition of a carry flag, the condition of the carry flag having been set by a previous arithmetic operation;
> performing an indexed load operation using the index register;
> ***wherein the conditional shift operation and the indexed load operation are performed during execution of a load-shift carry instruction***; and
> ***implementing a binary search of keys ordered in a table by executing the load-shift carry instruction.*** (emphasis added)

as in the present independent claims 1 and 6, from which claims 2-5 and 7- 19 depend. Like Cho, Narad et al., Islam et al., and Stuttard et al. include no reference to searching or binary searches. The searching in Goboyan et al. is with respect to fields of a packet, such as addresses, and involves search trees in address look-up engines (ALEs). The searches in the ALEs of Goboyan et al. are based "strictly on the root pointer, the search key and search key length it is

given." See column 9, lines 5-15 of Gobovan et al. This stands in contrast to *implementing a binary search of keys ordered in a table by executing the load-shift carry instruction,* as in the present independent claims 1 and 6. Moreover, as noted in the previous response, none of the combined references include any discussion of a carry flag, nor any load-shift carry instruction that performs a conditional shift operation on an index register based on the condition of a carry flag, the condition of the carry flag having been set by a previous arithmetic operation, and an indexed load operation using the index register.

For the above reasons, Applicants respectfully urge that the combinations of references cited with Cho in paragraphs 4 through 19 of the Office Action do not disclose or suggest all of the features of the present independent claims 1 and 6. Accordingly, the reference combinations in paragraphs 4 through 8 of the Office Action fail to support a *prima facie* case of obviousness under 35 U.S.C. 103 with respect to these independent claims. As to dependent claims 2-5 and 7-19, they each depend from claims 1 and 6, and are respectfully believed to be patentable over the cited references for at least the same reasons.

For these reasons, Applicants respectfully request that the rejections of the Examiner be withdrawn. Reconsideration of all pending claims is respectfully requested.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone the undersigned, Applicants' Attorney at 617-630-1131 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

David A. Dagg, Reg. No. 37,809
Attorney/Agent for Applicant(s)
Steubing McGuinness & Manaras LLP
125 Nagog Park Drive
Acton, MA 01720
(978) 264-6664

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